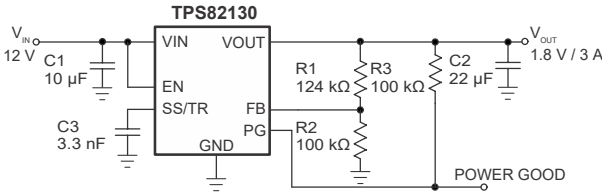
TPS82130 具有集成电感器的 17V 输入 3A 降压转换器 MicroSiP™ 电源模块

1 特性

- 3mm × 2.8mm × 1.5mm MicroSiP 封装
- 3V 至 17V 输入范围
- 3A 持续输出电流
- DCS-Control 拓扑
- 可实现轻负载效率的省电模式
- 20μA 工作静态电流
- 0.9V 至 6V 可调节输出电压
- 可实现最低压降的 100% 占空比
- 电源正常状态输出
- 具有跟踪功能的可编程软启动
- 热关断保护
- –40°C 至 125°C 工作温度范围
- 提供普通话数据表
- 使用 TPS82130 并借助 WEBENCH® Power Designer 创建定制设计

2 应用

- 工业应用
- 电信和网络应用
- 固态硬盘



1.8V 输出应用简化原理图

3 说明

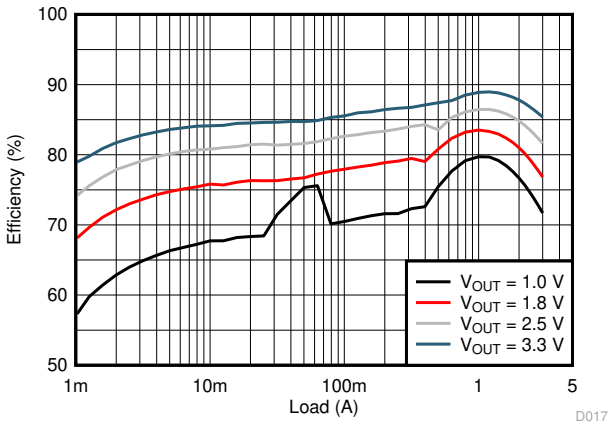
TPS82130 是一款 17V 输入 3A 降压转换器 MicroSiP 电源模块，经优化具有小解决方案尺寸和高效率等特性。该模块集成了一个同步降压转换器和一个电感器，以简化设计、减少外部元件数量并缩小 PCB 面积。该模块采用紧凑的薄型封装，适合通过标准表面贴装设备进行自动组装。

为了更大限度地提高效率，该转换器以 2MHz 的标称开关频率在 PWM 模式下工作，
并且会在轻负载电流条件下自动进入省电模式。在省电模式下，该器件以 20μA（典型值）的静态电流运行。通过使用 DCS-Control 拓扑，该器件可实现出色的负载瞬态性能和精确的输出稳压。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TPS82130	SIL（μSiL，8）	3.00mm × 2.80mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



12V 输入电压效率

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (October 2021) to Revision F (January 2023)	Page
• 添加了指向翻译后普通话数据表的超链接	1
• 更新的商标信息	1
• Added *Documentation Support* section	18

Changes from Revision D (November 2018) to Revision E (October 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式。	1

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5 Pin Configuration and Functions

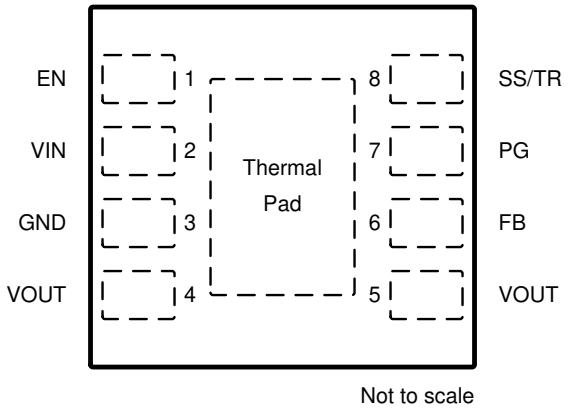

图 5-1. SIL 8-Pin µSiL Package (SIL0008C Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pulldown resistor of typically 400 kΩ when the device is disabled.
VIN	2	PWR	Input pin
GND	3		Ground pin
VOUT	4, 5	PWR	Output pin
FB	6	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
PG	7	O	Power-good open-drain output pin. A pullup resistor can be connected to any voltage less than 6 V. Leave this pin open if it is not used.
SS/TR	8	I	Soft start-up and voltage tracking pin. An external capacitor connected to this pin sets the internal reference voltage rising time.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

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6 规格

6.1 绝对最大额定值

		最小值	最大值	单位
引脚处的电压(1) (2)	VIN	-0.3	20	V
	EN、SS/TR	-0.3	V_{IN} + 0.3	
	PG、FB	–0.3	7	
	VOUT	0	7	
灌电流(1)	PG		10	mA
模块工作温度(1)		-40	125	°C
贮存温度(1)		–55	125	°C

(1) 超出那些最大绝对额定值下列出的压力可能会对器件造成永久损坏。这些仅为在压力额定值，并不表明器件在这些额定值下或者任何其它超过建议工作条件所标明的条件下可正常工作。长时间处于最大绝对额定情况下可影响设备的可靠性。
(2) 所有电压值都是相对于网络接地引脚的值。

6.2 ESD 等级

		值	单位
$V_{(ESD)}$ 静电放电	人体放电模式（HBM），符合 ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	充电器件模式（CDM），符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文件 JEP155 规定：500V HBM 可实现在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 规定：250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在自然通风温度范围内测得，除非另有说明。

		最小值	最大值	单位
V_{IN}	输入电压	3	17	V
V_{PG}	电源正常上拉电阻器电压		6	V
V_{OUT}	输出电压	0.9	6	V
I_{OUT}	输出电流	0	3	A
T_J	可实现 100,000 小时寿命的模块工作温度范围(1)	-40	110	°C

(1) 模块工作温度范围包含模块自温升和 IC 结温升。在存在高功率耗散的应用中，必须降低最高工作温度或最大输出电流。对于模块在 125 °C 温度下连续运行的应用，最长寿命减少至 50,000 小时。

6.4 热性能信息

热指标(1)		TPS82130（JEDEC 51-5）	TPS82130EVM-720	单位
$R_{\theta JA}$	结至环境热阻	58.2	46.1	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	9.4	9.4	°C/W
$R_{\theta JB}$	结至电路板热阻	14.4	14.4	°C/W
ψ_{JT}	结至顶部特征参数	0.9	0.9	°C/W
ψ_{JB}	结至电路板特征参数	14.2	14.0	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	21.3	21.3	°C/W

(1) 有关新旧热指标的更多信息，请参阅《半导体和 IC 封装热指标》应用报告。可以使用包含散热过孔的定制 PCB 设计（如可能）来改善 θ JA。

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6.5 电气特性

T_J = –40°C 至 125°C 且 V_{IN} = 3.0V 至 17V。除非另有说明，否则典型值是 T_J = 25°C 且 V_{IN} = 12V 条件下的典型值。

参数		测试条件		最小值	典型值	最大值	单位
电源							
I_Q	流入 VIN 的静态电流	无负载，器件未进行开关			20	35	μA
I_{SD}	流入 VIN 的关断电流	EN = 低电平			1.5	7.4	μA
V_{UVLO}	欠压闭锁阈值	V_{IN} 下降		2.6	2.7	2.8	V
		V_{IN} 上升		2.8	2.9	3.0	V
T_{JSD}	热关断阈值	T_J 上升			160		°C
		T_J 下降			140		°C
逻辑接口（EN）							
V_{IH}	高电平输入电压			0.9	0.65		V
V_{IL}	低电平输入电压				0.45	0.3	V
$I_{lkg(EN)}$	流入 EN 引脚的输入泄漏电流	EN = 高电平			0.01	1	μA
控制（SS/TR、PG）							
$I_{SS/TR}$	SS/TR 引脚拉电流			2.1	2.5	2.8	μA
V_{PG}	电源正常阈值	V_{OUT} 上升，以 V_{OUT} 标称值为基准		92%	95%	99%	
		V_{OUT} 下降，以 V_{OUT} 标称值为基准		87%	90%	94%	
$V_{PG,OL}$	电源正常低电平电压	I_{sink} = 2 mA			0.1	0.3	V
$I_{lkg(PG)}$	流入 PG 引脚的输入泄漏电流	V_{PG} = 1.8V			1	400	nA
输出							
V_{FB}	反馈调节电压	PWM 模式		785	800	815	mV
			T_J = 0°C 至 85°C	788	800	812	
		PSM	C_{OUT} = 22μF	785	800	823	
			C_{OUT} = 2 × 22μF，T_J = 0°C 至 85°C	788	800	815	
$I_{lkg(FB)}$	反馈输入泄漏电流	V_{FB} = 0.8 V			1	100	nA
	线调节	I_{OUT} = 1A，V_{OUT} = 1.8V			0.002		%/V
	负载调节	I_{OUT} = 0.5A 至 3A，V_{OUT} = 1.8V			0.12		%/A
电源开关							
$R_{DS(on)}$	高侧 FET 导通电阻	I_{SW} = 500mA，V_{IN} ≥ 6V			90	170	mΩ
		I_{SW} = 500mA，V_{IN} = 3V			120		
	低侧 FET 导通电阻	I_{SW} = 500mA，V_{IN} ≥ 6V			40	70	
		I_{SW} = 500mA，V_{IN} = 3V			50		
R_{DP}	压降电阻	100% 模式，V_{IN} ≥ 6V			125		mΩ
		100% 模式，V_{IN} = 3V			160		
I_{LIMF}	高侧 FET 开关电流限制	V_{IN} = 6V，T_A = 25°C		3.6	4.2	4.9	A
f_{SW}	PWM 开关频率	I_{OUT} = 1A，V_{OUT} = 1.8V			2.0		MHz

6.6 典型特性

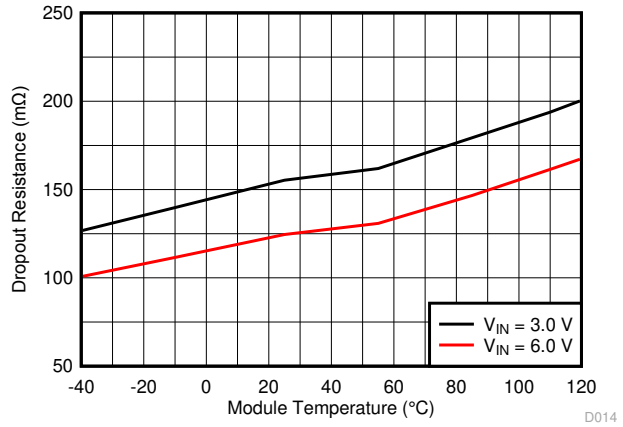

图 6-1. 压降电阻

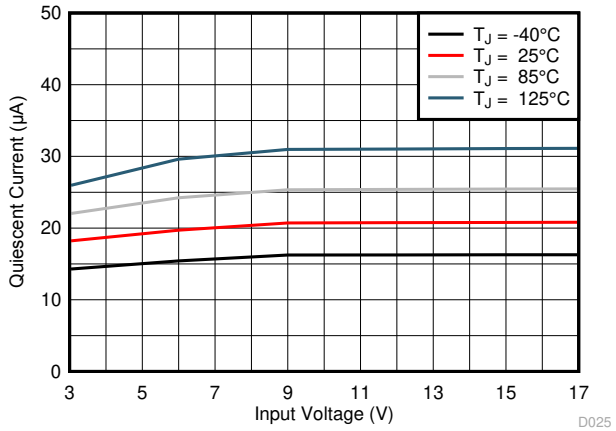

图 6-2. 静态电流

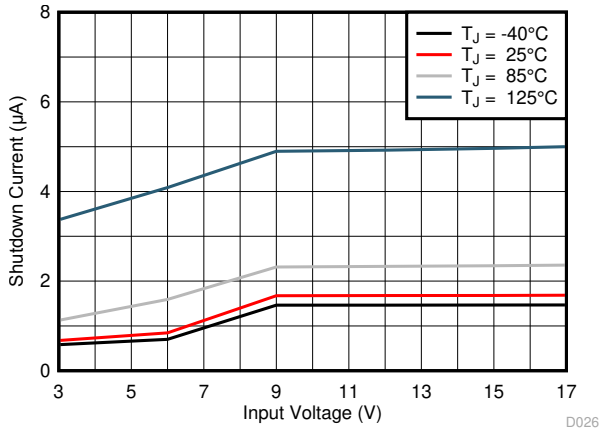

图 6-3. 关断电流

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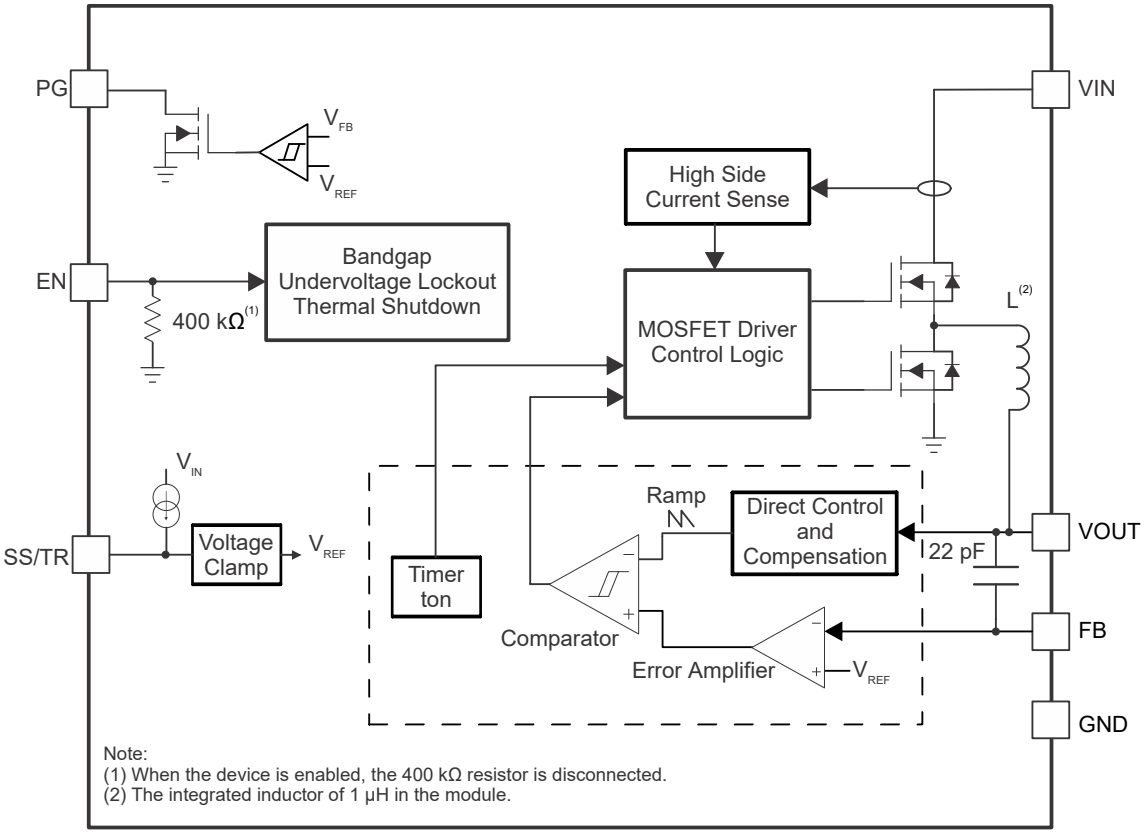
7 Detailed Description

7.1 概述

TPS82130 同步降压转换器 MicroSiP 电源模块基于 DCS-Control（可无缝转换到省电模式的直接控制）。DCS-Control 是一种高级调节拓扑，兼具磁滞和电压模式控制的优势。

DCS-Control 拓扑可以在中等负载至重负载条件下以 PWM（脉宽调制）模式运行，也可以在轻负载电流下以 PSM（省电模式）运行。在 PWM 模式下，该转换器以其 2.0MHz 的标称开关频率运行，并且在输入电压范围内的频率变化可控。随着负载电流的降低，转换器进入省电模式、降低开关频率并最大限度地降低 IC 的静态电流，可在整个负载电流范围内实现高效率。DCS-Control 使用单个构建块支持两种运行模式，因此可以从 PWM 无缝转换到 PSM，而不会影响输出电压。TPS82130 提供出色的直流电压调节和负载瞬态调节，并具有低输出电压纹波，可最大限度地减少对射频电路的干扰。

7.2 Functional Block Diagram



7.3 特性说明

7.3.1 PWM 和 PSM 运行

TPS82130 包含导通时间（t_{ON}）电路。在 PWM 和 PSM 模式下稳态运行时，可通过以下公式来估算 t_{ON}：

$$t_{ON} = 500ns \times \frac{V_{OUT}}{V_{IN}} \tag{1}$$

在 PWM 模式下，TPS82130 在连续导通模式（CCM）以及中高负载电流下以脉宽调制模式运行，其 t_{ON} 如方程式 1 所示。该 t_{ON} 电路可实现典型值为 2.0MHz 的 PWM 开关频率。只要输出电流高于电感器纹波电流（可通过方程式 2 进行估算）的一半，器件就会以 PWM 模式运行。

$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \tag{2}$$

为了在轻负载时保持高效率，器件会在负载电流降低时无缝进入省电模式。当负载电流小于电感器纹波电流的一半时，就会发生这种情况。在 PSM 模式下，转换器以更低的开关频率和最小静态电流运行来保持高效率。PSM 也基于 t_{ON} 电路。可通过以下公式来估算 PSM 模式下的开关频率：

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \tag{3}$$

在 PSM 模式下，输出电压略高于 PWM 模式下的标称输出电压。可通过增大输出电容来降低该影响。节 6.5 反映了 PSM 运行模式下的输出电压精度，针对 22μF 输出电容器提供。

对于非常小的输出电压，会保持大约 80ns 的绝对最小导通时间，以便限制开关损耗。工作频率因此低于其标称值，从而保持高效率。此外，在高占空比下，关断时间可以达到其最小值。在这种情况下，输出电压保持稳定。

当 V_{IN} 降低至比 V_{OUT} 高 15%（典型值）时，无论负载电流如何，TPS82130 都无法进入省电模式。器件在 PWM 模式下保持输出稳压状态。

7.3.2 低压降运行（100% 占空比）

TPS82130 通过进入 100% 占空比模式提供低输入到输出电压差动。在该模式下，高侧 MOSFET 开关始终开启。该特性在电池供电应用中特别有用，可通过充分利用整个电池电压范围来实现最长的运行时间。可通过以下公式来计算用于维持最小输出电压的最小输入电压：

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \tag{4}$$

其中

- R_{DP} = V_{IN} 和 V_{OUT} 之间的电阻，包括高侧 FET 导通电阻和电感器的直流电阻
- $V_{OUT(min)}$ = 负载可以接受的最低输出电压

7.3.3 开关电流限值

开关电流限值可防止器件出现高电感器电流和从电池或输入电压轨汲取过大的电流。在重负载/输出电路短路的情况下可能会出现过大的电流。如果电感器峰值电流在 30ns（典型值）的传播延迟后达到开关电流限值，高侧 FET 将关闭，低侧 FET 则会开启，从而减小电感器电流。

7.3.4 欠压锁定

为了避免器件在低输入电压下误操作，可进行欠压锁定，从而在电压低于 V_{UVLO} 时以 200mV 的迟滞关闭器件。

7.3.5 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. After the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 器件功能模式

7.4.1 启用和禁用（EN）

可以通过将 EN 引脚设置为逻辑高电平来启用器件。因此，如果 EN 引脚以典型值为 1.5μA 的关断电流拉低，则会强制实现关断模式。

当 EN 引脚为低电平时，内部 400kΩ 下拉电阻器连接到 EN 引脚。当 EN 引脚为高电平时，下拉电阻器断开。

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7.4.2 软启动（SS/TR）

内部电压钳位控制启动期间的输出电压斜率。这可以避免过大的浪涌电流并确保受控的输出电压上升时间。当 EN 引脚被拉高时，器件会在 55 μs（典型值）的延迟后开始开关，并且输出电压以由连接到 SS/TR 引脚的外部电容器控制的斜率上升。通过使用非常小的电容器或使 SS/TR 引脚悬空，可实现最快的启动时间。

TPS82130 能够启动至预偏置输出电容器。在预偏置启动期间，在内部电压钳位将输出电压设置为高于预偏置电压之前，两个功率 MOSFET 无法开启。

当器件处于关断、欠压锁定或热关断状态时，连接到 SS/TR 引脚的电容器由内部电阻器放电。从这些状态返回会导致新的启动序列。

7.4.3 电压跟踪（SS/TR）

SS/TR 引脚由另一个电压源从外部进行驱动，以实现输出电压跟踪。图 7-1 显示了应用电路。

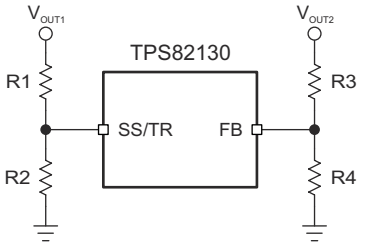

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图 7-1. 输出电压跟踪

当 SS/TR 引脚电压介于 50mV 和 1.2V 之间时，VOUT2 会跟踪 VOUT1，如方程式 5 所示。

$$\frac{V_{OUT2}}{V_{OUT1}} \approx 0.64 \times \frac{R2}{R1+R2} \times \frac{R3+R4}{R4} \tag{5}$$

当 SS/TR 引脚电压高于 1.2V 时，禁用电压跟踪，FB 引脚电压被调节为 0.8V。为了降低 SS/TR 引脚电压，器件不会从输出端灌入电流，因此，如果负载较轻，则导致的输出电压下降速度可能比 SS/TR 引脚电压慢。在使用外部电压驱动 SS/TR 引脚时，不要超过 SS/TR 引脚的额定电压，即 VIN + 0.3V。

有关跟踪和时序控制电路的详细信息，请参阅*《使用 TPS621 系列和 TPS821 系列进行时序控制和跟踪应用报告》*。

7.4.4 电源正常输出（PG）

该器件具有电源正常（PG） 输出输出高于标称电压的 95% 时，PG 引脚会变为高阻抗；输出电压低于标称电压的 90%（典型值）时，PG 引脚会被驱动为低电平。PG 引脚是开漏输出，其额定灌电流不超过 2mA。电源正常输出需要使用一个连接到任何低于 6V 的电压轨的上拉电阻器。

通过将 PG 信号连接到其他转换器的 EN 引脚，可以使用 PG 信号对多个电源轨进行时序控制。未使用 PG 引脚时，应将其保持悬空状态。表 7-1 显示了 PG 引脚逻辑。

表 7-1. 电源正常引脚逻辑

器件状态		PG 逻辑状态	
		高阻抗	低电平
启用（EN = 高电平）	$V_{FB} \geqslant V_{TH_PG}$	√	
	$V_{FB} \leqslant V_{TH_PG}$		√
关断（EN = 低电平）			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
热关断	$T_J > T_{SD}$		√
电源移除	$V_{IN} < 0.7V$	√	

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8 应用和实现

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

可通过元件选择来调节 TPS82130 的输出电压。以下部分介绍了外部元件的设计，通过使用典型应用作为参考来完成多个输入和输出电压选项的电源设计。

8.2 Typical Applications

8.2.1 1.8-V Output Application

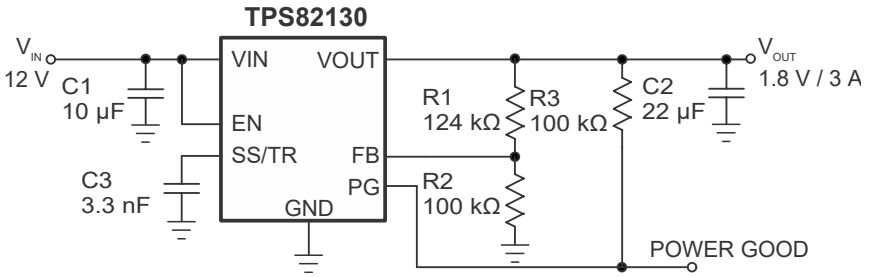

图 8-1. 1.8-V Output Application

8.2.1.1 设计要求

本设计示例使用以下参数作为输入参数。

表 8-1. 设计参数

设计参数	示例值
输入电压范围	12V
输出电压	1.8V
输出纹波电压	< 20mV
输出电流额定值	3A

下表提供了用于测量的元件。

表 8-2. 元件列表

基准	说明	制造商
C1	10µF，25V，X7R，±20%，尺寸 1206，C3216X7R1E106M160AE	TDK
C2	22µF，10V，±20%，X7S，尺寸 0805，C2012X7S1A226M125AC	TDK
C3	3300pF，50V，±5%，C0G/NP0，尺寸 0603，GRM1885C1H332JA01D	Murata
R1，R2，R3	标准	

8.2.1.2 详细设计过程

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.

2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 方程式 6:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \tag{6}$$

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. 图 8-1 shows the external resistor divider value for a 1.8-V output. Choose appropriate resistor values for other outputs.

In case the FB pin gets opened, the device clamps the output voltage at the VOUT pin internally to approximately 7 V.

8.2.1.2.3 Input and Output Capacitor Selection

For the best output and input voltage filtering, low-ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. A 10-µF or larger input capacitor is required. The output capacitor value can range from 22 µF up to more than 400 µF. Higher values are possible as well and can be evaluated through the transient response. TI recommends larger soft start times for higher output capacitances.

High capacitance ceramic capacitors have a DC bias effect, which have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.1.2.4 软启动电容器选型

SS/TR 引脚和 GND 之间连接的电容可实现对输出电压的启动斜率进行编程。2.5 µA 的恒定电流为外部电容器充电。可通过以下公式来计算实现输出电压的给定软启动时间所需的电容：

$$C_{SS/TR} = t_{SS/TR} \times \frac{I_{SS/TR}}{1.25V} \tag{7}$$

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8.2.1.3 应用性能曲线

T_A = 25°C，V_{IN} = 12V，V_{OUT} = 1.8V（除非另有说明）。

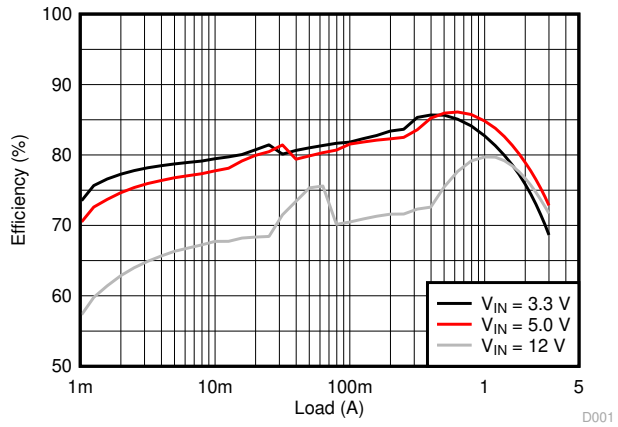


图 8-2. 效率（V_{OUT} = 1V）

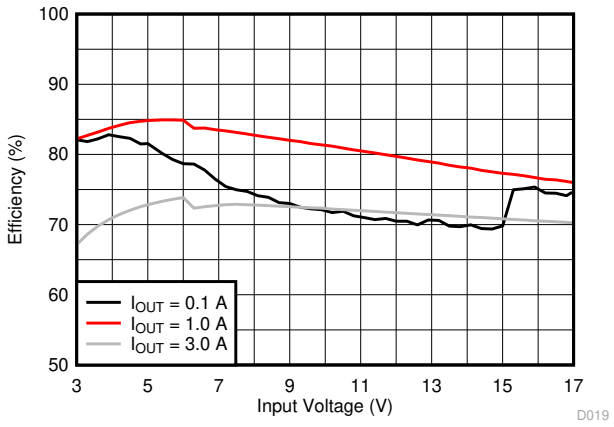


图 8-3. 效率（V_{OUT} = 1.0V）

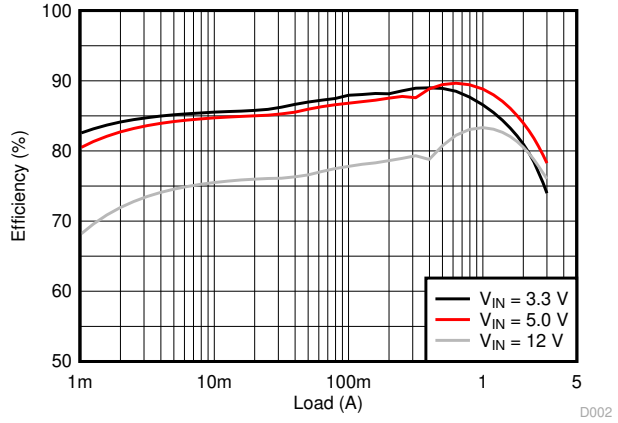


图 8-4. 效率（V_{OUT} = 1.8V）

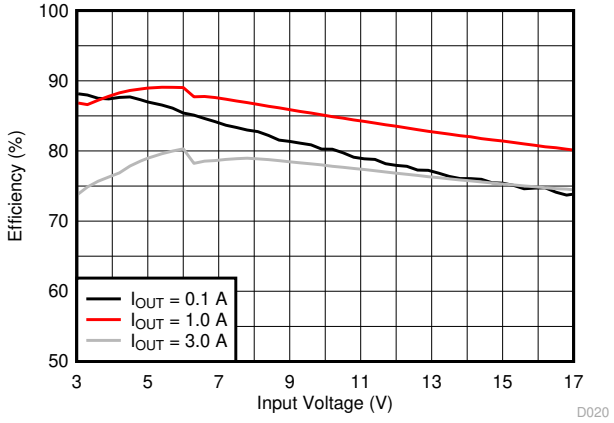


图 8-5. 效率（V_{OUT} = 1.8V）

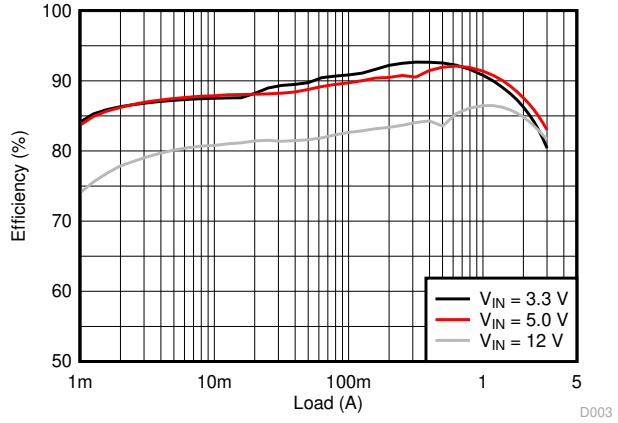


图 8-6. 效率（V_{OUT} = 2.5V）

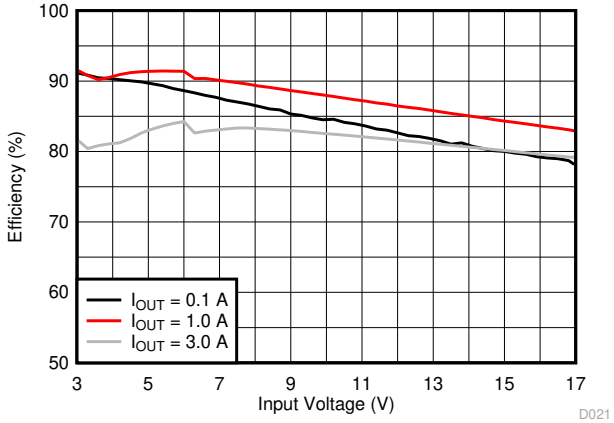


图 8-7. 效率（V_{OUT} = 2.5V）

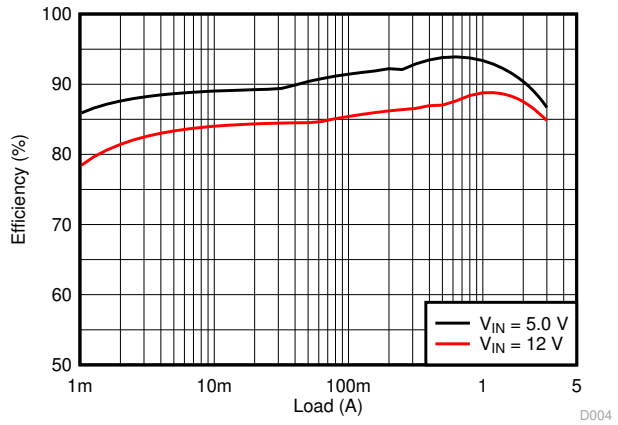


图 8-8. 效率（V_{OUT} = 3.3V）

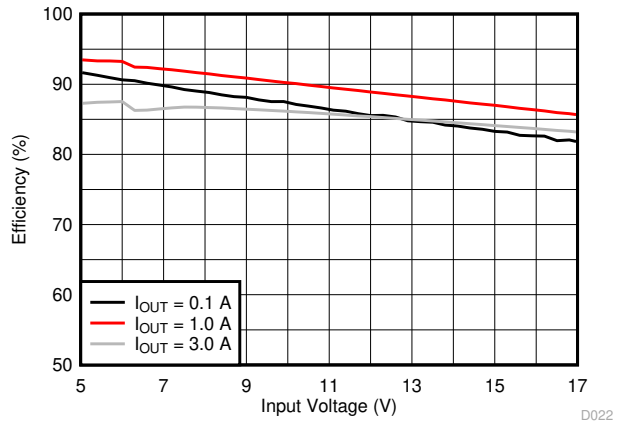


图 8-9. 效率（V_{OUT} = 3.3V）

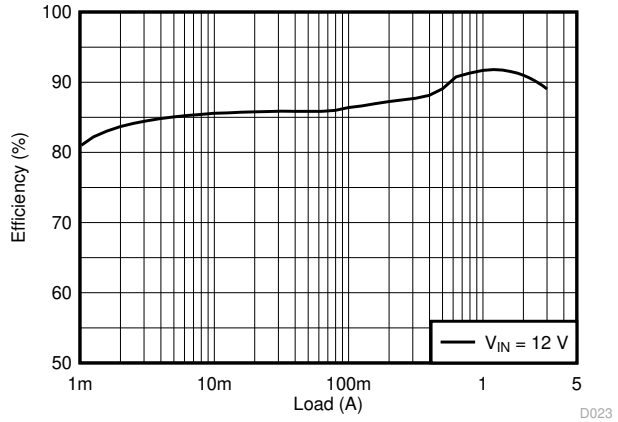


图 8-10. 效率（V_{OUT} = 5.0V）

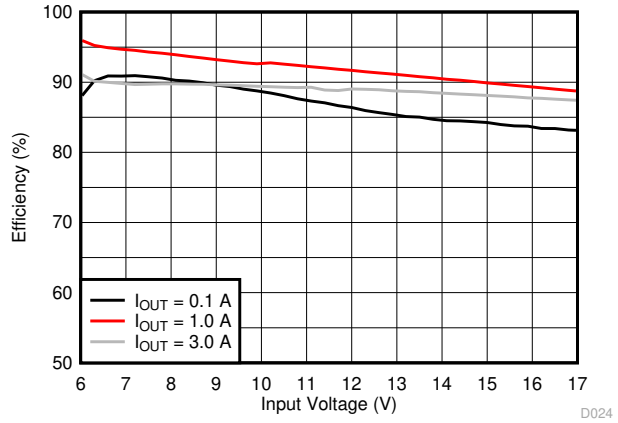
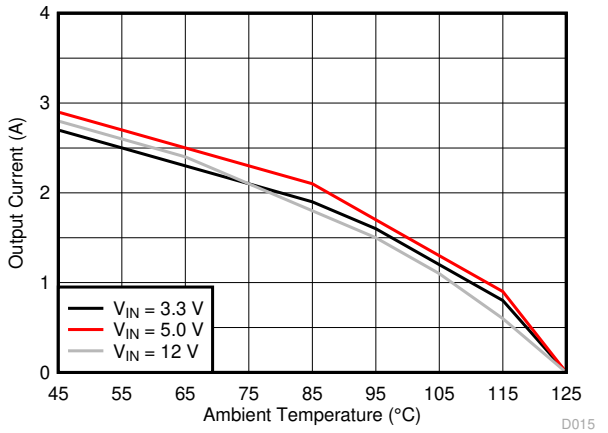
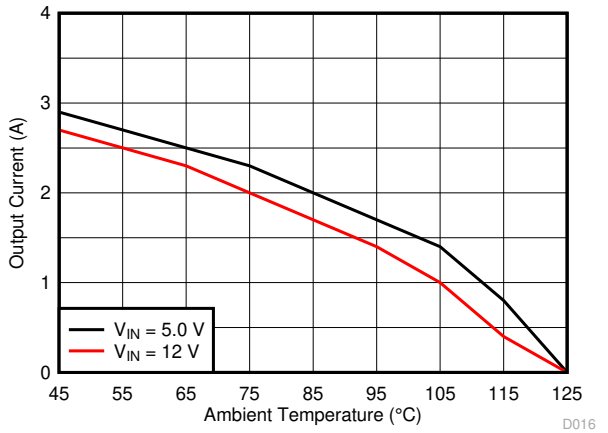


图 8-11. 效率（V_{OUT} = 5V）



V_{OUT} = 1.8 V　　θ_{JA} = 46.1°C/W

图 8-12. 热降额（V_{OUT} = 1.8V）



V_{OUT} = 3.3V　　θ_{JA} = 46.1°C/W

图 8-13. 热降额（V_{OUT} = 3.3V）

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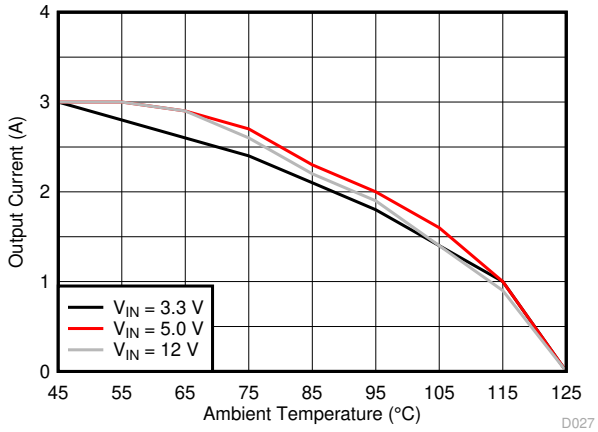
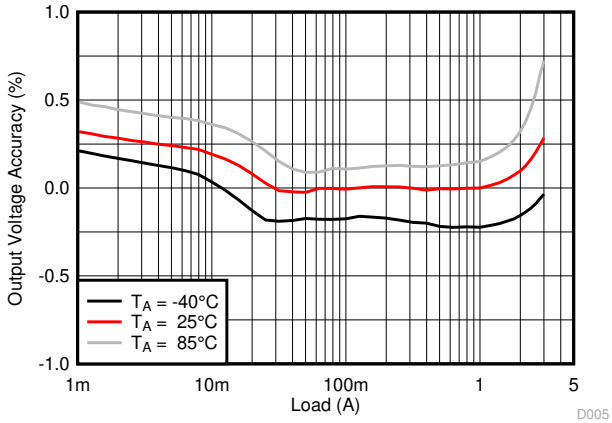
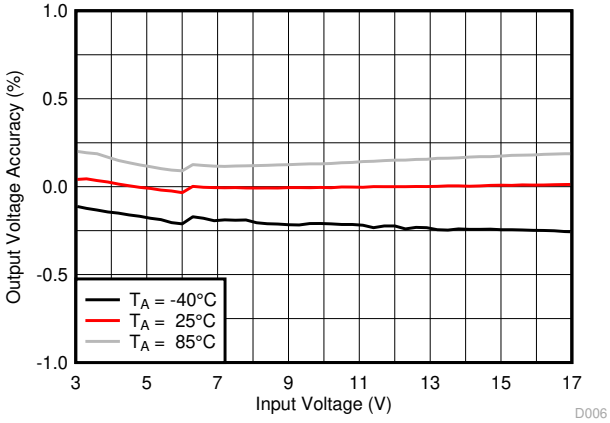


图 8-14. 热降额（V_{OUT} = 1.0V）



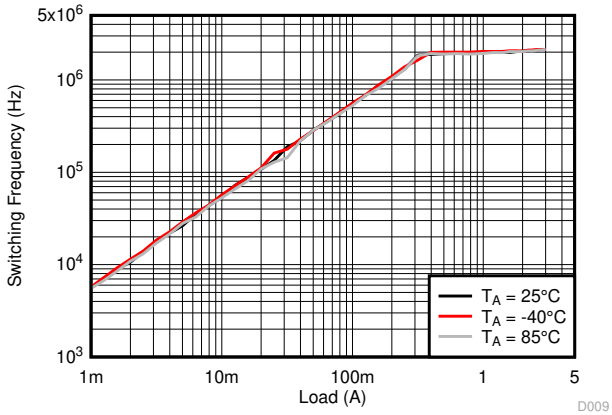
V_{IN} = 12V

图 8-15. 负载调节



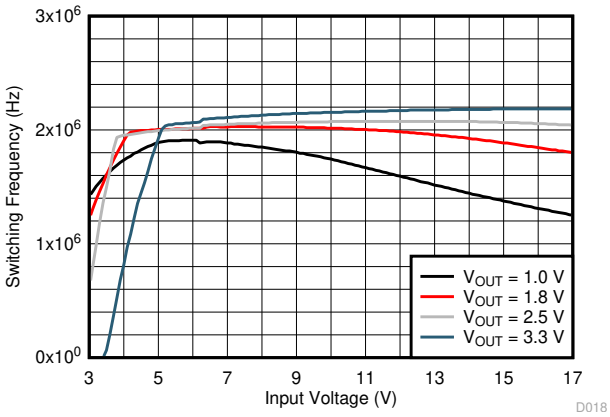
I_{OUT} = 1A

图 8-16. 线路调节



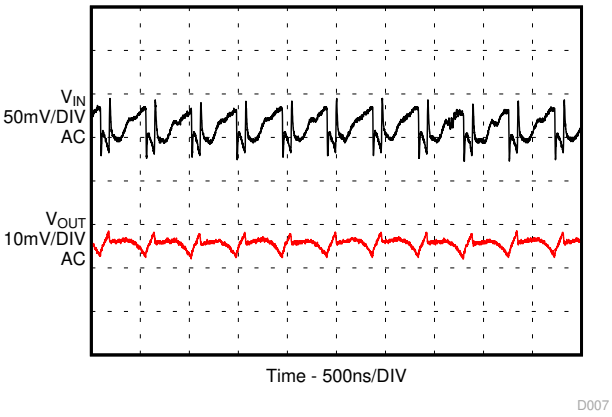
V_{OUT} = 1.8 V　　V_{IN} = 12V

图 8-17. 开关频率



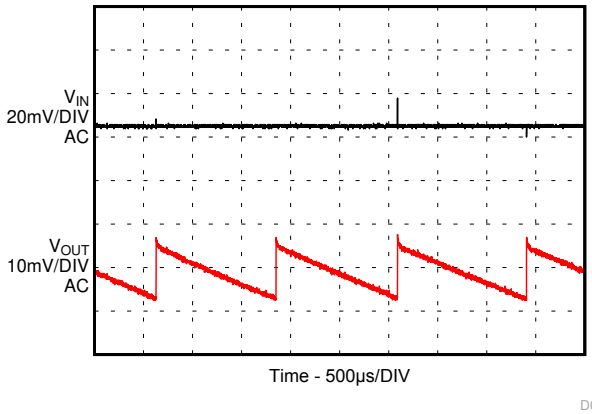
I_{OUT} = 1A

图 8-18. 开关频率



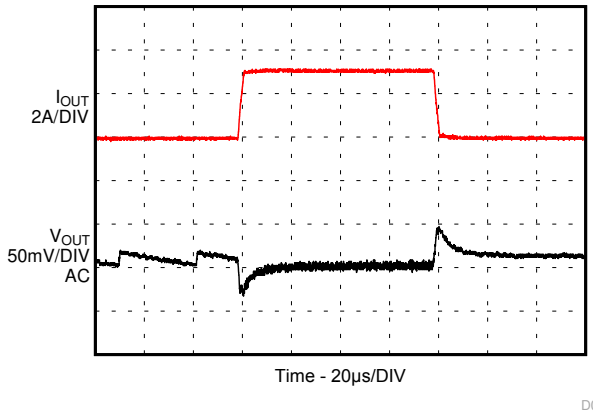
I_{OUT} = 3A

图 8-19. PWM 模式下的输入和输出纹波



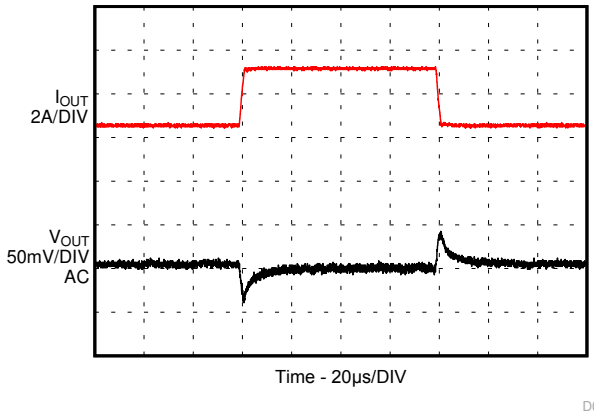
空载

图 8-20. PSM 模式下的输入和输出纹波



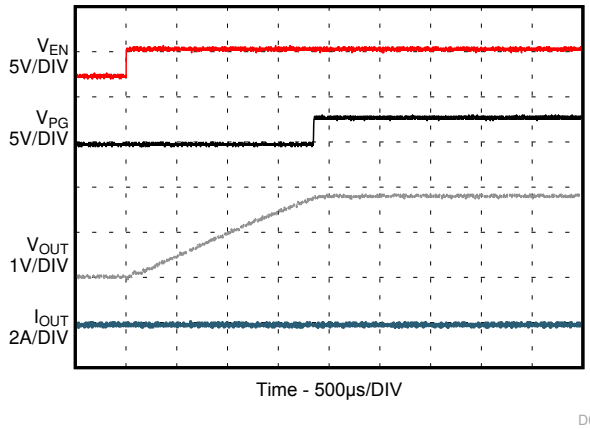
I_{OUT} = 0A 至 3A，1A/µs

图 8-21. 负载瞬态



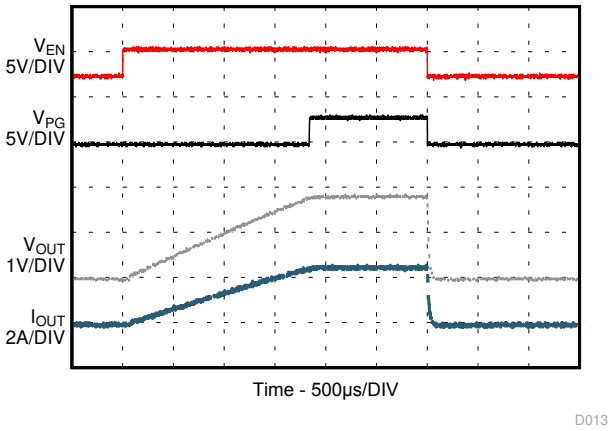
I_{OUT} = 0.5A 至 3A，1A/µs

图 8-22. 负载瞬态



空载

图 8-23. 在空载条件下启动



R_{OUT} = 0.68 Ω

图 8-24. 电阻负载下的启动/关断

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8.3 电源建议

这些器件可在 3V 至 17V 的输入电源电压范围内工作。可通过以下公式来计算 TPS82130 的平均输入电流：

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \tag{8}$$

请确保电源的额定电流足以满足应用需求。

8.4 布局

8.4.1 Layout Guidelines

- TI recommends placing all components as close as possible to the IC. The input capacitor placement specifically must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad must be connected to bottom or internal layer ground planes using vias.
- Refer to 图 8-25 for an example of component placement, routing, and thermal design.

8.4.2 布局示例

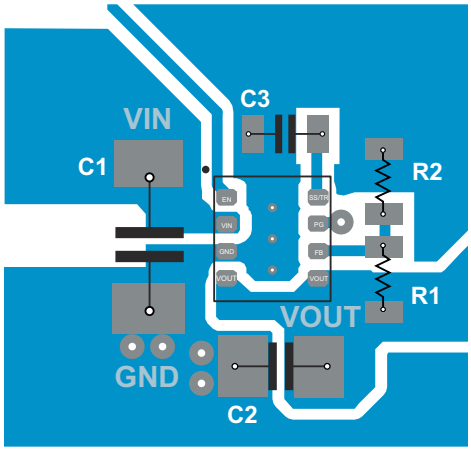

图 8-25. TPS82130 PCB 布局

8.4.3 Thermal Consideration

The output current of the TPS82130 must be derated when the device operates in a high ambient temperature or delivers high output power. The amount of current derating is dependent upon the input voltage, output power, PCB layout design, and environmental thermal condition. Care must especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS82130 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the TPS82130 to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82130, apply the typical efficiency stated in this data sheet to the desired application condition to find the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report* and *Semiconductor and IC Package Thermal Metrics application report*.

9 器件和文档支持

9.1 器件支持

9.1.1 开发支持

9.1.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.1.1.2 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS82130 device with the WEBENCH Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application report*
- Texas Instruments, *Sequencing and Tracking With the TPS621-Family and TPS821-Family application report*

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 商标

MicroSiP™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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9.7 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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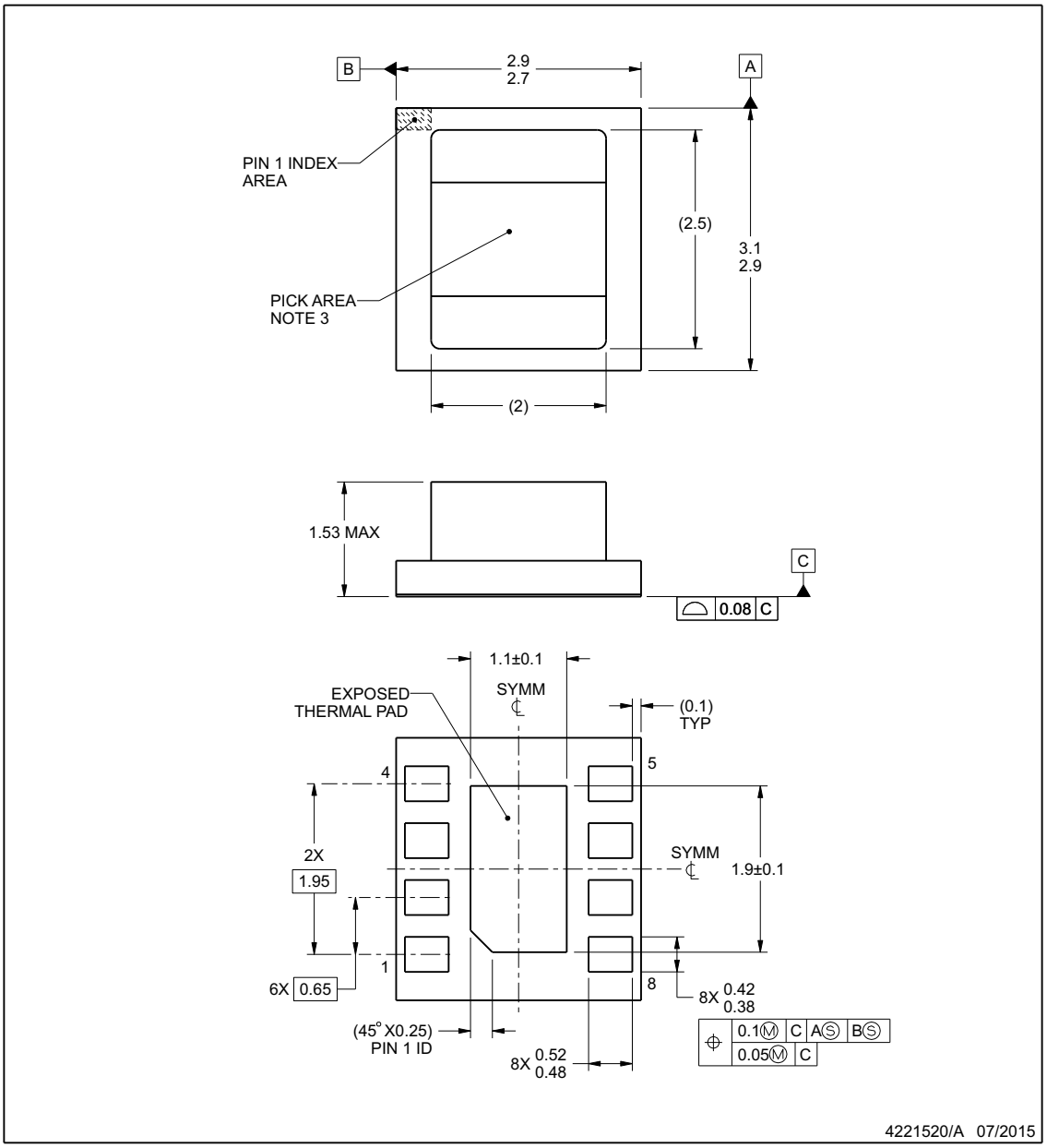
PACKAGE OUTLINE

SIL0008D

MicroSiP™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

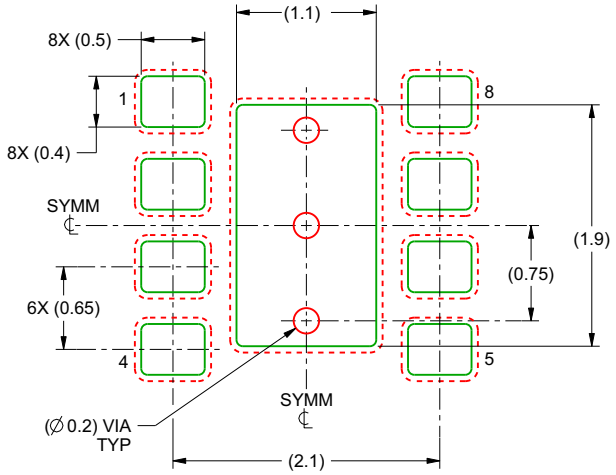
www.ti.com

EXAMPLE BOARD LAYOUT

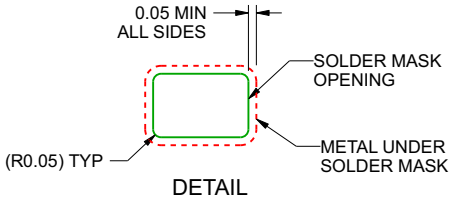
SIL0008D

MicroSiP ™ - 1.53 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X



DETAIL
NOT TO SCALE

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NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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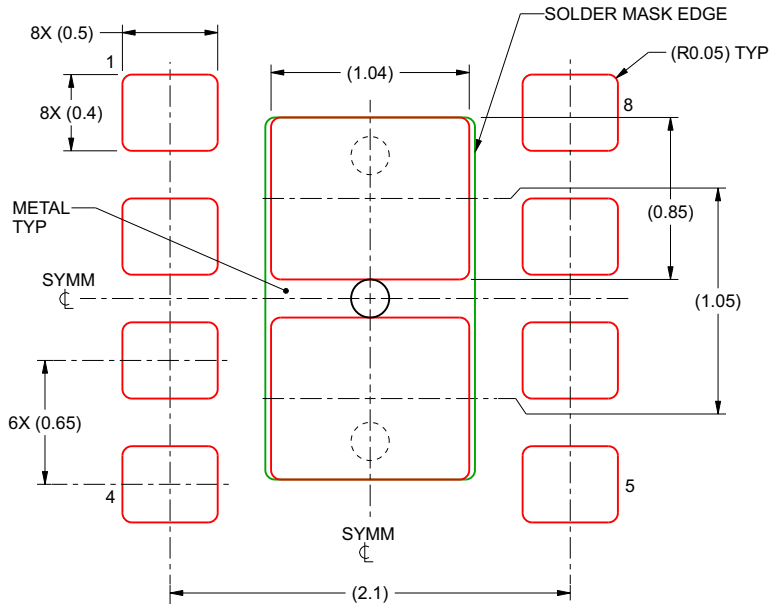
EXAMPLE STENCIL DESIGN

SIL0008D **MicroSiP ™ - 1.53 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221520/A 07/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS82130SILR	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILR.A	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILR.B	Active	Production	uSiP (SIL) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS82130SILT	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILT.A	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	Yes	NIAU	Level-2-260C-1 YEAR	-40 to 125	H6
TPS82130SILT.B	Active	Production	uSiP (SIL) | 8	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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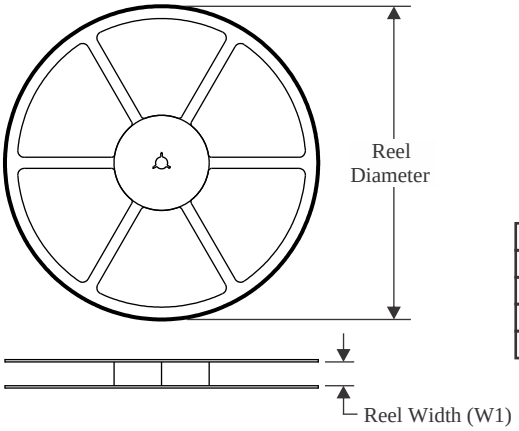
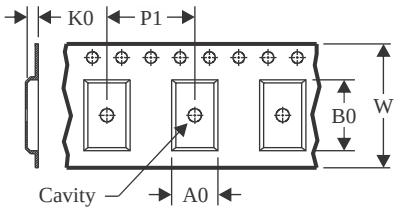
TAPE AND REEL INFORMATION

REEL DIMENSIONS

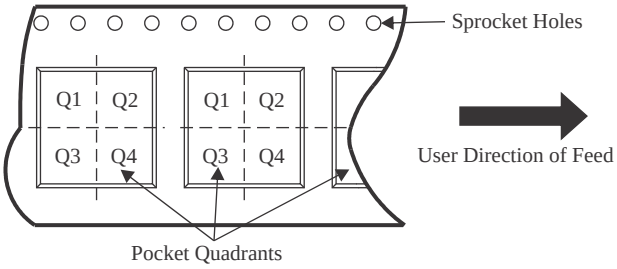


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

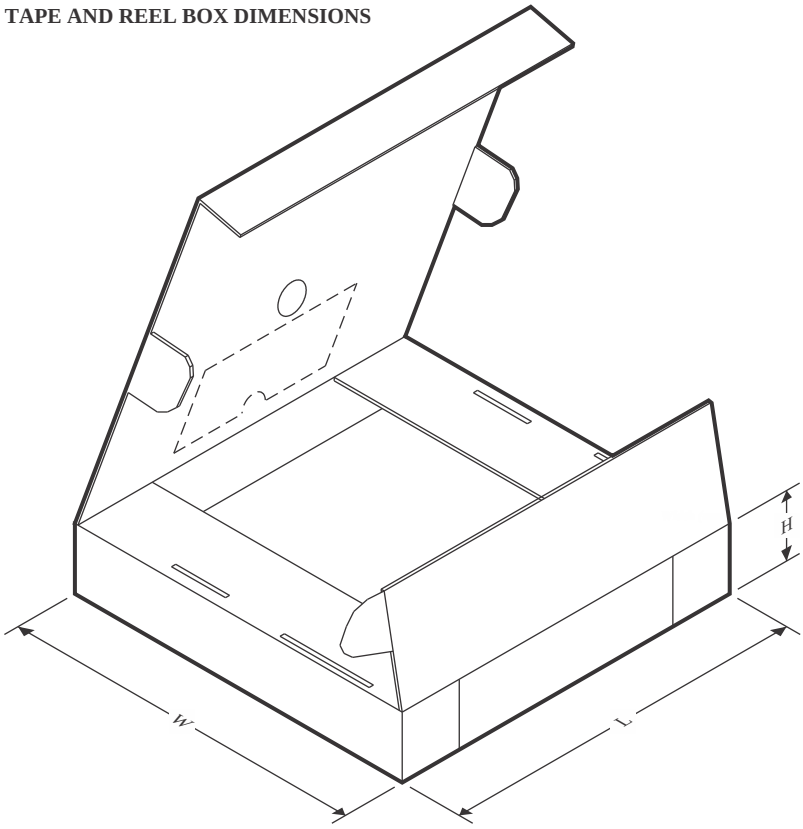
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82130SILR	uSiP	SIL	8	3000	330.0	12.4	3.05	3.25	1.68	8.0	12.0	Q1
TPS82130SILT	uSiP	SIL	8	250	178.0	13.2	3.05	3.25	1.68	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82130SILR	uSiP	SIL	8	3000	383.0	353.0	58.0
TPS82130SILT	uSiP	SIL	8	250	223.0	194.0	35.0

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